November 13, 2018

Verilog Applications Hand's on Workshop

Two days workshop was conducted for the pre final year students on "The applications of Verilog" on 5th and 7th November '18. The key note address was delivered by Prof Gangadaraiah SL, was an educative one which gave glimpses of the various challenges and the plethora of opportunities in the Integrated circuit design process.

During the workshop duration, the students were introduced to industry relevant concepts like: Finite state machines, IP core generation, FIFO design with hardware, Parity generator, CRC checker and Wallace tree multiplier. The onus of the workshop training was shared by Dr Ipsitha, Prof Shalini V, Prof Kavitha, Prof Raghuveer CM and Prof Vasudeva G.

Highlights

01

Hand's on workshop on application of Verilog beyond curriculum

02

Technical talk on Machine learning

Technical Talk on Machine Learning

On 15th November, department is organizing a technical talk on Machine Learning for final year and pre final year students.